Sub E1

CLAIMS:

1. A method for enhancing data retention of a floating gate transistor comprising:

forming a floating gate over a substrate, the floating gate having an inner first portion and an outer second portion; and

providing conductivity enhancing impurity in the inner first portion to a greater concentration than conductivity enhancing impurity in the outer second portion.

2. The method of claim 1, wherein the forming of the floating gate comprises forming the inner first portion and the outer second portion to comprise polysilicon.

3. The method of claim 1, wherein the floating gate has a thickness, and the forming of the floating gate comprises forming the inner first portion to comprise at least 25 percent of the floating gate thickness.

4. The method of claim 1, wherein the floating gate has a thickness, and the forming of the floating gate comprises forming the inner first portion to comprise between about 25 to 75 percent of the floating gate thickness.

5. The method of claim 1, wherein the providing of conductivity enhancing impurity in the inner first portion comprises doping the inner first portion to a dopant concentration greater than or equal to $1 \times 10^{18} cm^{-3}$.

6. The method of claim 1, wherein the providing of conductivity enhancing impurity in the inner first portion comprises doping the inner first portion to a dopant concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$, with the outer second portion having a dopant concentration of less than $1 \times 10^{18} cm^{-3}$.

7. The method of claim 1, wherein:

the forming of the floating gate comprises forming a first layer of polysilicon over the substrate, the first layer defining the inner first portion, and after the forming of the first layer forming a second layer of polysilicon, the second layer defining the outer second portion.

8. method of claim 1, wherein

the forming of the floating gate comprises forming a first layer of polysilicon over the substrate, the first layer defining the inner first portion, and after the forming of the first layer forming a second layer of polysilicon, the second layer defining the outer second portion; and

intermediate the forming of the first and second layers, providing the conductivity enhancing impurity in the inner first portion to a dopant concentration of greater than or equal to about 1 x $10^{18}cm^{-3}$.

9. A method of forming a floating gate transistor comprising:

forming a first layer of conductively doped semiconductive material over a semiconductive substrate;

forming a second layer of substantially undoped semiconductive material over the first layer;

forming a third layer comprising dielectric material over the second layer;

forming a fourth layer comprising conductive material over the third layer; and

forming a floating gate transistor comprising the first, second, third, and fourth layers.

10. method of claim 9, wherein the first and second layers comprise a floating gate having a thickness, and the forming of the first and second layers comprise forming the first layer to occupy at least 25 percent of the floating gate thickness.

11. The method of claim 9, wherein the first and second layers comprise a floating gate having a thickness, and the forming of the first and second layers comprise forming the first layer to occupy less than 75 percent of the floating gate thickness.

12. The method of claim 9, wherein the forming of the first layer comprises forming the first layer to have a dopant concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

13. The method of claim 9, wherein the forming of the first layer comprises:

forming a layer of polysilicon over the substrate; and

doping the polysilicon layer with phosphorous dopant material to a concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

14. method of claim 9, wherein:

the first and second layers comprise a floating gate having a thickness, and the forming of the first and second layers comprise forming the first layer to occupy less than 75 percent of the floating gate thickness; and

the forming of the first layer comprises forming the first layer to have a dopant concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

15. A method of forming a floating gate comprising:

forming a first material over a substrate, the first material having a first average grain size;

forming a second material over the first material, the second material having a second average grain size, the second average grain size being larger than the first average grain size; and

providing the first and second materials into a desired floating gate shape.

16. The method of claim 15, wherein the forming of the first material comprises forming conductively doped polysilicon to have a sheet resistance of between 300 ohm/sq. and 400 ohm/sq..

17. The method of claim 15, wherein

the forming of the first material comprises forming conductively doped polysilicon to have a sheet resistance of between 300 ohm/sq. and 400 ohm/sq.; and

the forming of the second material comprises forming polysilicon to have a sheet resistance greater than 400 ohm/sq.

18. The method of claim 15, wherein the forming of the first material comprises forming conductively doped polysilicon to have a dopant concentration greater than or equal to about $1 \times 10^{18} cm^{-3}$.

19. The method of claim 15, wherein the forming of the second material comprises forming the second material directly atop the first material.

20. The method of claim 15, wherein the forming of the second material comprises forming the second material directly atop the first material, the first and second materials having a combined thickness of less than or equal to about 1000 Angstroms, the first material having an individual thickness of less than about 75 percent of the combined thickness.

21. A method of forming a floating gate transistor comprising:

forming a floating gate over a substrate, the floating gate comprising a first silicon-containing volume having a first grain boundary area per unit volume, and a second silicon-containing volume over the first silicon-containing volume having a second grain boundary area per unit volume, the second grain boundary area per unit volume being less than the first grain boundary area per unit volume;

forming a dielectric layer over the second silicon-containing volume; and

forming a conductive line over the dielectric layer to provide a floating gate transistor.

22. The method of claim 21, wherein the forming of the dielectric layer comprises forming an oxide layer atop the second silicon-containing volume.

23. The method of claim 21, wherein the forming of the floating gate comprises:

forming a first layer of conductively doped polysilicon over the substrate, the first layer constituting the first silicon-containing volume and having a dopant concentration of greater than or equal to about 1 x $10^{18}cm^{-3}$ and a sheet resistance of between about 300 ohm/sq. and 400 ohm/sq..

24. The method of claim 21, wherein the forming of the floating gate comprises:

forming a first layer of conductively doped polysilicon over the substrate, the first layer constituting the first silicon-containing volume and having a dopant concentration of greater than or equal to about 1 x $10^{18}cm^{-3}$ and a sheet resistance of between about 300 ohm/sq. and 400 ohm/sq.; and

after forming the first layer, forming a second layer of polysilicon over the first layer, the second layer constituting the second silicon-containing volume and having a dopant concentration less than about 1 x $10^{18}cm^{-3}$ and a sheet resistant greater than 400 ohm/sq..

Sub E1

25. A method of forming a floating gate transistor comprising:

forming a first layer of polysilicon over a substrate to a first thickness;

doping the first layer to a degree sufficient to define a sheet resistance of between 300 ohm/sq. and 400 ohm/sq.;

after the doping, forming a second layer of polysilicon over the first layer of polysilicon to a second thickness;

oxidizing the substrate to form a first oxide layer over the second layer of polysilicon;

forming a layer of nitride over the first oxide layer;

oxidizing the substrate to form a second oxide layer over the layer of nitride;

forming a third layer of polysilicon over the second oxide layer; and

etching at least some of the layers to provide a floating gate transistor over the substrate.

√ 26. The method of claim 25, wherein the first and second thicknesses are substantially the same.

√ 27. The method of claim 25, wherein the first and second thicknesses are different.

28. method of claim 25, wherein the first and second thicknesses comprise an aggregate thickness and the first thickness constitutes less than or equal to about 75 percent of the aggregate thickness.

29. The method of claim 25, wherein the first thickness is less than about 550 Angstroms.

30. The method of claim 25, wherein the first thickness is between 450 Angstroms and 550 Angstroms.

31. The method of claim 25, wherein the forming of the second layer of polysilicon comprises forming the layer to have a sheet resistance which is greater than the sheet resistance of the first layer of polysilicon.

32. A floating gate transistor comprising:

a substrate; and

a floating gate over the substrate having an inner first portion and an outer second portion, the inner first portion being disposed proximate the substrate and the outer second portion being disposed over the inner first portion, the inner first portion containing a concentration of conductivity enhancing impurity which is greater than a concentration of conductivity enhancing impurity contained by the outer second portion;

a dielectric layer disposed over the outer second portion;

a conductive line disposed over the dielectric layer; and

source/drain regions laterally proximate the floating gate.

33. The floating gate transistor of claim 32, wherein the inner first portion contains an impurity concentration of greater than or equal to about 1 x $10^{18}cm^{-3}$.

34. The floating gate transistor of claim 32, wherein the inner first portion contains an impurity concentration of greater than or equal to about 1 x $10^{18}cm^{-3}$, and the outer second portion contains an impurity concentration of less than 1 x $10^{18}cm^{-3}$.

35. The floating gate transistor of claim 32, wherein the floating gate has a thickness, and the inner first portion constitutes less than about 75 percent of the floating gate thickness.

36. The floating gate transistor of claim 32, wherein the floating gate has a thickness, and the inner first portion constitutes less than or equal to about 50 percent of the floating gate thickness.

37. A floating gate transistor comprising:

a substrate;

a floating gate over the substrate comprising a first material having a first average grain size and a second material disposed over the first material and having a second average grain size which is larger than the first average grain size;

a dielectric layer disposed over the second material;

a conductive line disposed over the dielectric layer; and

source/drain regions laterally proximate the floating gate.

38. The floating gate transistor of claim 37, wherein the first material has a sheet resistance of less than about 400 ohm/sq..

39. The floating gate transistor of claim 37, wherein the first and second materials define an aggregate thickness and the first material occupies less than 75 percent of ~~the aggre~~gate thickness.

40. [redacted] floating gate transistor of [redacted] 37, wherein the first and second material have individual respective thicknesses and the first material thickness is less than the second material thickness.

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